Universitatea Transilvania din Braşov
Facultatea Inginerie Electrică şi Ştiinţa Calculatoarelor (IESC)
Departamentul Electronică şi Calculatoare (EC)

Poz. Postului 44
Disciplinele postului:
Inginerie software şi aplicaţii în comunicaţiile de date,
Inginerie software
Sisteme distribuite şi de timp real
Microcontrolere
Programare în JAVA
Programarea calculatoarelor şi limbaje de programare

# FIŞA DE VERIFICARE A ÎNDEPLINIRII STANDARDELOR UNIVERSITĂŢII

Postul: Şef lucrări (pe perioadă nedeterminată), poziţia 44,
publicat în Monitorul Oficial al României[1] nr. 1251 din data de 24.11.2022

Candidat: Cătălin Bogdan CIOBANU Data naşterii 13.04.1983
Funcţia actuală: Şef de Lucrări Instituţia Universitatea Transilvania Braşov

1. Studii universitare (licenţă şi masterat)

| Nr. crt. | Instituţia de învăţământ superior şi facultatea | Domeniul | Perioada | Titlul acordat |
|---|---|---|---|---|
| 1 | Universitatea Transilvania Braşov, Facultatea de Inginerie Electrică şi Ştiinţa Calculatoarelor | Profilul Electronic, specializarea Electronică Aplicată | 2001-2006 | Inginer Diplomat |
| 2 | Technische Universiteit Delft, Olanda, Faculty of Electrical Engineering, Mathematics and Computer Science | Computer Engineering | 2006-2007 | Master of Science |

2. Studii de doctorat

| Nr. crt. | Instituţia organizatoare de doctorat | Domeniul | Perioada | Titlul ştiinţific acordat |
|---|---|---|---|---|
| 1 | Technische Universiteit Delft, Olanda | Computer Engineering | 2007-2013 | Doctor |

3. Studii şi burse postdoctorale (stagii de cel puţin 6 luni)

| Nr. crt. | Instituţia | Domeniul/ Specializarea | Perioada | Tipul de bursă |
|---|---|---|---|---|
| 1 | Chalmers University of Technology, Suedia | Computer Engineering | 2013-2015 | Contract pe proiect european |
| 2 | University of Amsterdam, Olanda | Systems and Networking (SNE) lab, Informatics Institute | 2015-2018 | Contract pe proiect european |

[1] Numărul documentului se completează numai în cazul posturilor pe perioadă nedeterminată.

4. Standarde minimale ale universității

| Post didactic<br>(se menține în tabel numai postul pentru care se candidează) | Realizări conform standardelor proprii ale Universității |
|---|---|
| Șef de lucrări | **(i) Articol în revistă cotată ISI WoS cu SRI > 0.5, ca prim autor**<br>**C.B. Ciobanu**, G. Gaydadjiev, C. Pilato and D. Sciuto, The Case for Polymorphic Registers in Dataflow Computing, International Journal of Parallel Programming, December 2018, pp. 1185-1219, https://doi.org/10.1007/s10766-017-0494-1<br>Online: https://link.springer.com/article/10.1007/s10766-017-0494-1<br>SRI: 0.608<br><br>**(ii) Alte articole ISI WoS cu SRI > 0.5**<br>1. A. L. Machidon, O. M. Machidon, C. B. Ciobanu, and P. L. Ogrutan, "Accelerating a Geometrical Approximated PCA Algorithm Using AVX2 and CUDA," Remote Sensing, vol. 12, no. 12, p. 1918, Jun. 2020 https://doi.org/10.3390/rs12121918<br>Online: https://www.mdpi.com/2072-4292/12/12/1918/htm<br>SRI: 4.509 (2019) ; 5-Year Impact Factor: 5.001 (2019)<br><br>2. G. Stramondo, **C.B. Ciobanu**, C. de Laat, A.L. Varbanescu, Designing and Building Application-Centric Parallel Memories, in Concurrency and Computation: Practice and Experience, https://doi.org/10.1002/cpe.5485<br>Online: https://onlinelibrary.wiley.com/doi/full/10.1002/cpe.5485<br>SRI: 1.447 (2019), 1.268 (5 year)<br><br>3. Pnevmatikatos, K. Papadimitriou, T. Becker, P. Bohm, A. Brokalakis, K. Bruneel, **C.B. Ciobanu**, T. Davidson, G. Gaydadjiev, K. Heyse, W. Luk, X. Niu, I. Papaefstathiou, D. Pau, O. Pell, C. Pilato, M. D. Santambrogio, D. Sciuto, D. Stroobandt, T. Todman, E. Vansteenkiste, FASTER: Facilitating Analysis and Synthesis Technologies for Effective Reconfiguration, Elsevier Journal on |

Microprocessors and Microsystems (MICPRO), pp. 321-338, November 2014, ISSN: 0141-9331, eISSN: 1872-9436
https://doi.org/10.1016/j.micpro.2014.09.006
SRI: 1.161 (2019), 1.119 (5 year)

4. Ramirez, F. Cabarcas, B.H.H. Juurlink, M. Alvarez, F. Sanchez, A. Azevedo, C.H. Meenderinck, **C.B. Ciobanu**, S. Isaza, G. N. Gaydadjiev, The SARC Architecture, IEEE Micro, pp. 16-29, Vol. 30, Nr. 5, ISSN: 0272-1732, https://doi.org/10.1109/MM.2010.79
Online:
https://ieeexplore.ieee.org/document/5567090
SRI: 3.172 (2019), 2.682 (5 year) Q1

**(iii) Alte articole publicate**

1. D. Crăciun, N. Bălăceanu, A. Chiriță, **C.B. Ciobanu**, Robotic Arm Control via Hand Movements, International Symposium on Electronics and Telecommunications 2022 (ISETC 2022), pp. 1-4, Timișoara, România, Noiembrie 2022

2. A. Machidon, **C.B. Ciobanu**, O. Machidon, P. Ogrutan, On Parallelizing Geometrical PCA Approximation, 2019 18th RoEduNet Conference: Networking in Education and Research (RoEduNet), pp. 1-6, Galați, România, October 2019

3. L. Stornaiuolo, M. Rabozzi, M. Santambrogio, D. Sciuto, G. Stramondo, **C.B. Ciobanu** and A.L. Varbanescu, HLS Support for Polymorphic Parallel Memories, 26th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI SoC), pp. 143-148, Verona, Italy, October 2018

4. G. Stramondo, **C. B. Ciobanu**, A. L. Varbanescu, C. de Laat, Towards Application-Centric Parallel Memories, Euro-Par 2018: Parallel Processing Workshops, pp. 481-493, Turin, Italy, August 2018

5. **C. B. Ciobanu**, G. Stramondo, A. L. Varbanescu, A. Brokalakis, A. Nikitakis, L. Di Tucci, M. Rabozzi, L. Stornaiuolo, M. Santambrogio, G. Chrysos, C. Vatsolakis, C. Georgios, and D. Pnevmatikatos, EXTRA: An Open Platform for

Reconfigurable Architectures, 2018 International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS XVIII, pp. 220-229, Samos Island, Greece, July 2018, https://doi.acm.org/10.1145/3229631.3236092

6. **C. B. Ciobanu**, G. Stramondo, C. de Laat and A. L. Varbanescu, MAX-PolyMem: High-Bandwidth Polymorphic Parallel Memories for DFEs, 2018 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), pp. 107-114, Vancouver, Canada, May 2018, https://doi.org/10.1109/IPDPSW.2018.00025

7. Kulkarni, P. Bahrebar, D. Stroobandt, G. Stramondo, **C. B. Ciobanu** and A. L. Varbanescu, A NoC-based Custom FPGA Configuration Memory Architecture for Ultra-fast Micro-reconfiguration, 2017 International Conference on Field Programmable Technology (ICFPT), pp. 203-206, Melbourne, Australia, December 2017

8. M. Rabozzi, R. Brondolin, G. Natale, E. Del Sozzo, M. Huebner, A. Brokalakis, **C.B. Ciobanu**, D. Stroobandt, M. Santambrogio., A CAD Open Platform for High Performance Reconfigurable Systems in the EXTRA Project, 2017 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), pp. 368-373, Bochum, Germany, July 2017

9. D. Stroobandt, **C.B. Ciobanu**, M. Santambrogio, G. Figueiredo, A. Brokalakis, D. Pnevmatikatos, M. Huebner, T. Becker, A. Thom., An Open Reconfigurable Research Platform as Stepping Stone to Exascale High-performance Computing, Proceedings of the Conference on Design, Automation & Test in Europe (DATE), pp 416-421, Lausanne, Switzerland, March 2017

10. D. Stroobandt, A.L. Varbanescu, **C.B. Ciobanu**, M. Al Kadi, A. Brokalakis, G. Charitopoulos, T. Todman, X. Niu, D. Pnevmatikatos, A. Kulkarni, E. Vansteenkiste, W. Luk, M. Santambrogio, D. Sciuto, M. Huebner, T. Becker, G. Gaydadjiev, A. Nikitakis, A. Thom, EXTRA: Towards the exploitation of eXascale technology for reconfigurable architectures, 2016 11th

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|---|---|
| | International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), pp. 1-7, Tallinn, June 2016.<br><br>11. G. Stramondo, A. Varbanescu, **C.B. Ciobanu**, The Case for Custom Parallel Memories: an Application-centric Analysis, Second International Workshop on Heterogeneous High-performance Reconfigurable Computing (H2RC), Salt Lake City, UT, USA, 2016<br><br>12. **C.B. Ciobanu**, A. L. Varbanescu, D. Pnevmatikatos, G. Charitopoulos, X. Niu, W. Luk, M. D. Santambrogio, D. Sciuto, M. A. Kadi, M. Huebner, T. Becker, and G. Gaydadjiev, A. Brokalakis, A. Nikitakis, A. J. W. Thom, E. Vansteenkiste, D. Stroobandt, EXTRA: Towards an Efficient Open Platform for Reconfigurable High Performance Computing, 2015 IEEE 18th International Conference on Computational Science and Engineering, pp. 339-342, Porto, Portugal, October 2015<br><br>13. G. Smaragdos, C. Davies, C. Strydis, I. Sourdis, **C.B. Ciobanu** , O. Mencer, C. De Zeeuw, Real-Time Olivary Neuron Simulations on Dataflow Computing Machines, Proceedings of International Supercomputing Conference (ISC 2014), pp. 487-497, Leipzig, Germany, June 2014<br><br>14. **C.B. Ciobanu**, G.N. Gaydadjiev, C. Pilato, D. Sciuto, Dataflow Computing with Polymorphic Registers, Proceedings of the 2013 International Conference<br>on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS 2013), pp. 314-321, Samos, Greece, July 2013<br><br>15. **C.B. Ciobanu**, D.N. Pnevmatikatos, K.D. Papadimitriou, G.N. Gaydadjiev, FASTER Run-time Reconfiguration Management, Proceedings of the 27th International Conference on Supercomputing (ICS 2013), pp. 463-464, Eugene, Oregon, USA, June 2013<br><br>16. **C.B. Ciobanu**, G. N. Gaydadjiev, Separable 2d Convolution with Polymorphic Register Files, Proceedings of the 2013 Conference on Architecture of Computing Systems (ARCS |

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17. K. Papadimitriou, C. Pilato, D. Pnevmatikatos, M.D. Santambrogio, **C.B. Ciobanu**, T. Todman, T. Becker, T. Davidson, X. Niu, G. N. Gaydadjiev, W. Luk, D. Stroobandt, Novel Design Methods and a Tool Flow for Unleashing Dynamic Reconfiguration, Proceedings of the 15 th International Conference on Computational Science and Engineering (CSE 2012), pp. 391-398, December 2012

18. **C.B. Ciobanu**, G. Kuzmanov, G. N. Gaydadjiev, Scalability Study of Polymorphic Register Files, Proceedings of the international conference on Digital System Design (DSD 2012), pp. 803-808, Cesme, Izmir, Turkey, September 2012

19. **C.B. Ciobanu**, G. Kuzmanov, G. N. Gaydadjiev, On Implementability of Polymorphic Register Files, Proceedings of the 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC 2012), pp. 1-6, York, UK, July 2012

20. **C. B. Ciobanu**, G. Kuzmanov, A. Ramirez, G. N. Gaydadjiev, Parallel Access Schemes for Polymorphic Register Files: Motivation Study, Advanced Computer Architecture and Compilation for Embedded Systems (ACACES), pp. 127-130, Fiuggi, Italy, 2011

21. **C. B. Ciobanu**, X. Martorell, G. Kuzmanov, A. Ramirez, G. N. Gaydadjiev, Scalability Evaluation of a Polymorphic Register File: a CG Case Study, Proceedings of the 2011 Conference on Architecture of Computing Systems (ARCS 2011), pp. 13-25, Como, Italy, 2011

22. **C. B. Ciobanu**, G. Kuzmanov, A. Ramirez, G. N. Gaydadjiev, A Polymorphic Register File for Matrix Operations, Proceedings of the 2010 International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS 2010), pp. 241-249, Samos, Greece, 2010

23. C. B. Ciobanu, G. Kuzmanov, A. Ramirez, G. N. Gaydadjiev, A Polymorphic Register File Architecture, Advanced Computer Architecture and Compilation for Embedded Systems (ACACES), pp. 245-248, Terrassa, Spain, 2009

24. D. Theodoropoulos, **C. B. Ciobanu**, G. Kuzmanov, Wave Field Synthesis for 3D Audio: Architectural Prospectives, ACM International Conference on Computing Frontiers, pp. 127-136, Ischia, Italy, 2009

25. B. Spinean, **C. B. Ciobanu**, G. Kuzmanov, G. N. Gaydadjiev, Design Considerations for a Domain Specific Vector Microarchitecture, in proceedings of PRORISC 2007, pp. pp. 178-184, Veldhoven, The Netherlands, 2007

26. **C. B. Ciobanu**, B. Spinean, G. Kuzmanov, G. N. Gaydadjiev, Customized Vector Instruction Set Architecture, proceedings of PRORISC 2007, pp. 128-137, Veldhoven, The Netherlands, 2007

**(iv) Volum(e) de specialitate publicat(e) în edituri recunoscute național**

1. **C.B. Ciobanu**, Customizable Register Files for Multidimensional SIMD architectures, Delft University of Technology, 2013, ISBN 978-94-6186-121-4

2. L. Stornaiuolo, M. Rabozzi, M. D. Santambrogio, D. Sciuto, **C. B. Ciobanu**, G. Stramondo, A. L. Varbanescu, Building High-Performance, Easy-to-Use Polymorphic Parallel Memories with HLS, capitol în VLSI-SoC: Design and Engineering of Electronics Systems Based on New Computing Paradigms, Springer, Cham, 2019, ISBN 978-3-030-23424-9

3. **C.B. Ciobanu**, Introducere în Proiectarea Sistemelor Încorporate, Editura Universității Transilvania din Brașov, 2022, ISBN 978-606-19-1564-4

**(v) Media anilor studii licență: 9,76**, [9,52 media anilor de studii+10,00 media la examenul de licență/diplomă)/2]

Candidat,

Ciobanu